4.5V-100V Vin, 0.6A, High Efficiency Synchronous Step-down DCDC Converter with Programmable Frequency

FEATURES

- Wide Input Range: 4.5V-100V
- 0.6A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 750mΩ High-Side and 500mΩ Low-Side Power MOSFETs
- Pulse Frequency Modulation (PFM) with 100uA Quiescent Current in Sleep Mode
- 4ms Internal Soft-start Time
- Adjustable Frequency 300KHz to 800KHz
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Cycle-by-Cycle Current Limiting
- Over-Voltage Protection
- Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- E-Tools
- E-bike, Scooter
- GPS Tracker

DESCRIPTION

The SCT2A10A is 0.6A synchronous buck converters with wide input voltage, ranging from 4.5V to 100V, which integrates an 750mΩ high-side MOSFET and a 500mΩ low-side MOSFET. The SCT2A10A, adopting the constant-

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to Market

Revision 1.1: Add application waveforms

Revision 1.2: Update R1 and R2 calculation value in page 11

Revision 1.3: Update figure 8

DEVICE ORDER INFORMATION

L=NP QI AN	L= G=CAI =NGE C	L= G=CA BO NELPEK
SCT2A10ASTE	A10A	8-Lead Plastic ESOP

1 For Tape & Reel, Add Suffix R (e.g. SCT2A10ASTER).

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

AO NELPEK	I E	I =T	Q EP
VIN, EN	-0.3	105	V
BOOT	-0.3	111	V
SW	-1	105	V
BOOT-SW	-0.3	6	V
FB, RT	-0.3	6	V
Ambient temperature T_A	-40	85	°C
Operating junction temperature T_J(2)	-40	125	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

Bec a 4 Ha L e A OKL

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. ij t apro du b] u t ضـ l mic l oml t ce o Junction temperat 1

BST	7	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

L=N=I APAN	ABE EPEK	I E	I =T	Q EP
V_{IN}	Input voltage range	4.5	100	V
V_{OUT}	Output voltage range	0.8	24	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

L=N=I APAN	ABE EPEK	I E	I =T	Q EP
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

L=N=I APAN	PDANI =HI APNE	B ,H	Q EP
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45.8	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2A10A is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2A10A. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_J=-40°C~125°C, typical value is tested under 25°C.

OUI KH	L=N=I APAN	PAOP K EPEK	I E PUL I =T	Q EP
L a O				
V_{IN}	Operating input voltage		4.5 100	V

V

OUI KH	L=N=I APAN	PAOP K EPEK	I E PUL I =T			Q EP
R_{DSON_L}	Low-side MOSFET on-resistance			500		mΩ
Naba a a H						
V_{REF}	Reference voltage of FB		0.792	0.8	0.808	V
A a O b						
V_{EN_H}	Enable high threshold			1.21		V
V_{EN_L}	Enable low threshold			1.05		V

$I_{EN\_}$ labl

TYPICAL CHARACTERISTICS

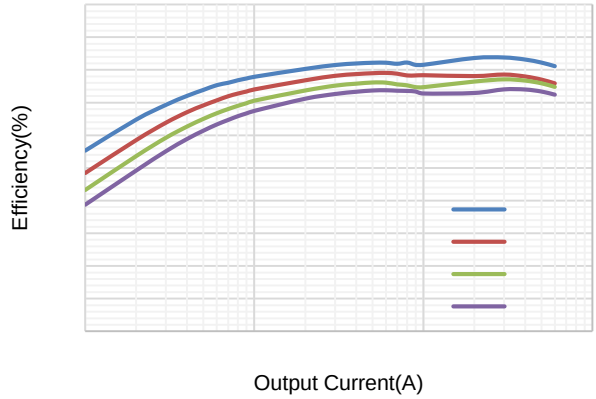

Figure 2. Efficiency vs Load Current (Vout=5V)

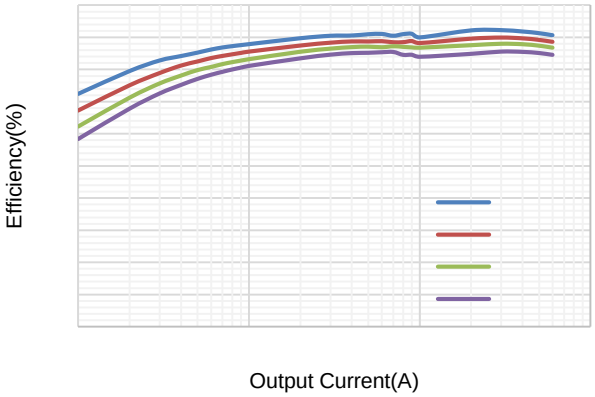

Figure 3. Efficiency vs Load Current (Vout=12V)

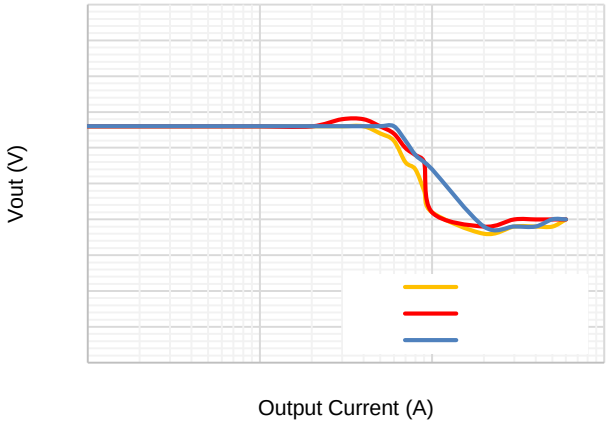

Figure 4. Load Regulation (Vout=12V)

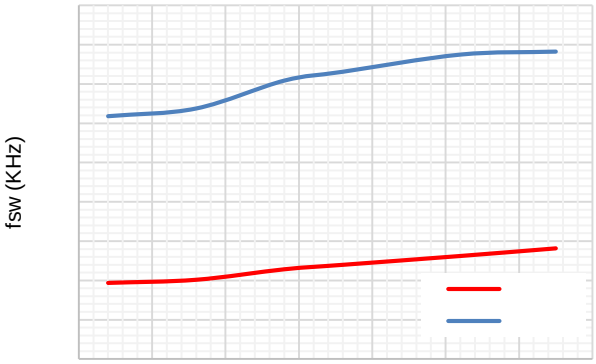

Figure 5 Frequency vs Temperature

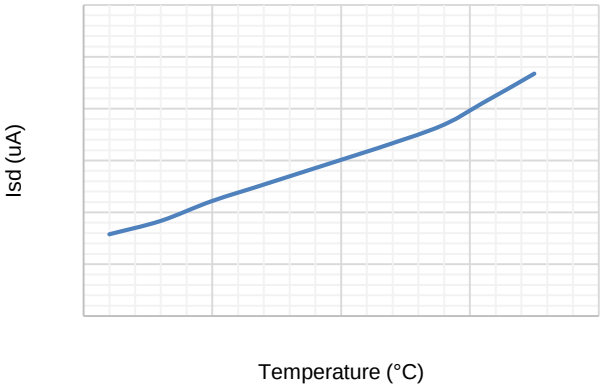

Figure 6. Shut-down Current vs Temperature

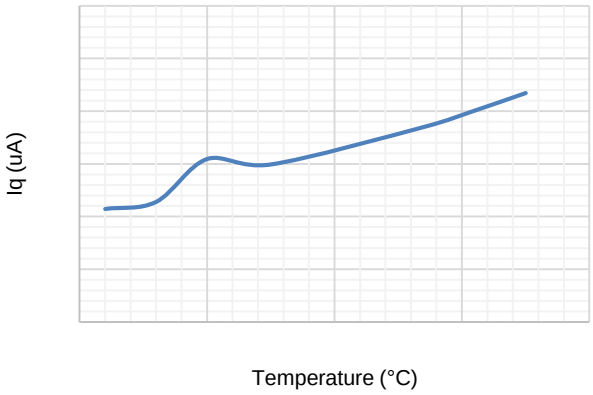

Figure 7. Iq vs Temperature

FUNCTIONAL BLOCK DIAGRAM

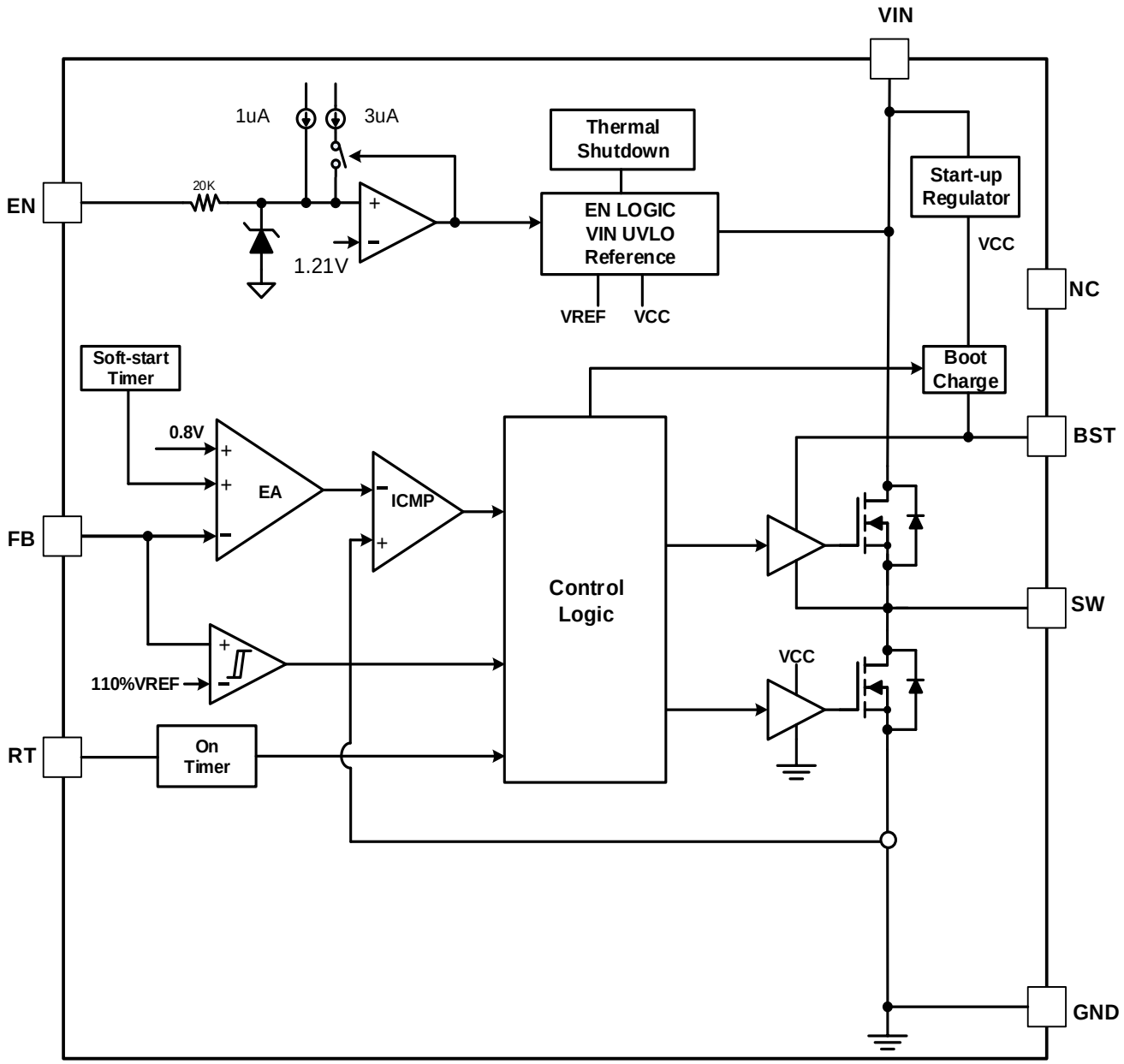

Figure 8. Functional Block Diagram

OPERATION

K a ea

The SCT2A10A is a 4.5V-100V input, 0.6A output, internal-compensated synchronous buck converter with built-in 750mΩ Rdson high-side and 500mΩ Rdson low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The switching frequency is programmable from 300kHz to 800KHz with resistor setting to optimizes either the power efficiency or the external components' sizes. The SCT2A10A features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PFM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 100uA under no load non-switching condition to achieve high efficiency at light load.

The SCT2A10A has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2A10A full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

K Pe a l a

The SCT2A10A employs Constant-On-Time Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, the high-side MOSFET (Q1) is turned on for a fixed interval and the inductor current rises to charge up the output voltage. When the high-side MOSFET (Q1) is turned off and the low-side MOSFET (Q2) is turned on after a dead time duration. When sensed the valley current passing on the low side MOSFET lower than the COMP current threshold, the device turns on Q1 and the low-side MOSFET (Q2) turns off. Based on Vin and Vout voltage, the device predicts required off-time and turns off low-side MOSFET Q2. This repeats on cycle-by-cycle based.

A a Q a R

(1)

(2)

Where

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1uA
I_2=3uA
V_{ENR}=1.21V
V_{EMF}=1.05V

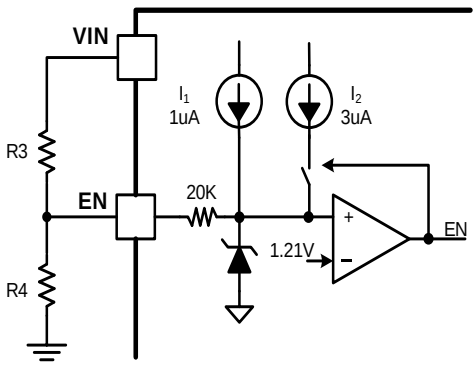

Figure 9. System UVLO by enable divide

K R ca

The SCT2A10A regulates the internal reference voltage at 0.8V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

(3)

where

R_{FB_TOP} is the resistor connecting the output to the FB pin.

R_{FB_BOT} is the resistor connecting the FB pin to the ground.

E a O b O

The SCT2A10A integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 1.05V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

O e de c B a a

The switching frequency of the SCT2A10A is set by placing a resistor between RT pin and the ground.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 300KHz to 800KHz. RT pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

Where,

fsw is switching clock frequency

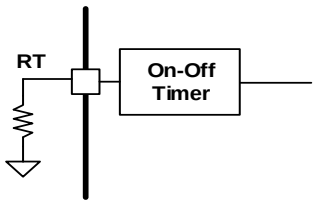

Figure 10. Setting Frequency

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R ca Nac

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

K a a He e De l a

The inductor current is monitored during low-side MOSFET Q2 on. The SCT2A10A implements over current protection with cycle-by-cycle limiting low-side MOSFET valley current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

K a ca L a e

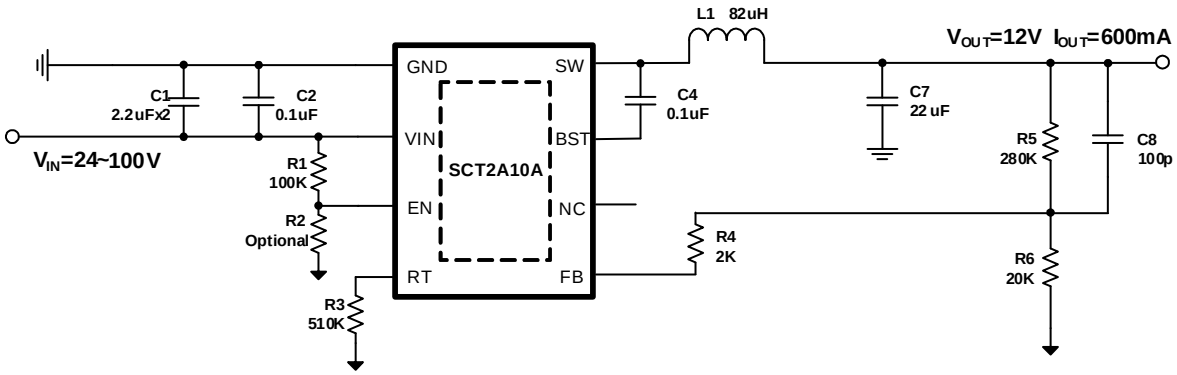
The SCT2A10A implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Pda Od

The SCT2A10A protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 167C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 132C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

P e = e e



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Input Voltage	48V Normal 24V to 100V
Output Voltage	12V
Maximum Output Current	600mA
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 60mA to 540mA load step	ΔVout = 400mV

K R ca

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 5 to calculate R5.

R_{KQP}	N_1	N_2
3.3 V	63.5 KΩ	20 KΩ
5 V	105 KΩ	20 KΩ
12 V	280 KΩ	20 KΩ
24 V	580 KΩ	20 KΩ

(5)

where:

V_{REF} is the edback reference voltage, typical 0.8V

Q a R ca H K

An extern vider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 32.7V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 26.5 V (stop or disable). Use Equation 6 and Equation 7 to calculate the values 599 kΩ and 22.6 kΩ of R_1 and R_2 resistors.

Where

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=1uA
I_2=3uA
V_{ENR}=1.21V
V_{EMF}=1.05V

E Oa a e

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 8.

V_{OUT} is the output voltage
V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

(9)

Where

L_{MIN} is the minimum inductance required
f_{sw} is the switching frequency
V_{OUT} is the output voltage
$V_{IN(max)}$ is the maximum input voltage
$I_{OUT(max)}$ is the maximum DC load current
LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 10 and equation 11.

(10)

(11)

Where

I_{LPEAK} is the inductor peak current
I_{OUT} is the DC load current
I_{LPP} is the inductor peak-to-peak current
I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor valley current can increase up to the switch current limit of the device which is typically 0.8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 0.8A. Because of the maximum $I_{LVALLEY}$ limited by device, the maximum output current that the SCT2A10A can deliver also depends on the inductor current ripple. Thus, th ų Ж husOUT

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 12.

(12)

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

(13)

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 14 and the maximum input voltage ripple occurs at 50% duty cycle.

(14)

For this example, three 2.2μF, X7R ceramic capacitors rated for 100V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

e Oa a e

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 25V or higher voltage rating.

K e Oa a e

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 15 desired.

(15)

Where

Δ is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
$V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

= e e S ab

Vin=48V, Vout=12V, unless otherwise noted

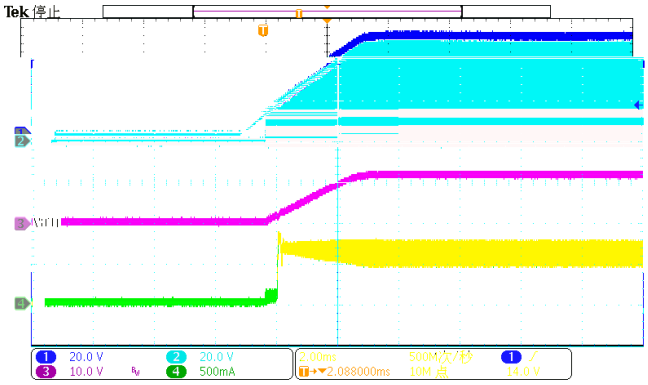

Figure 12. Power up

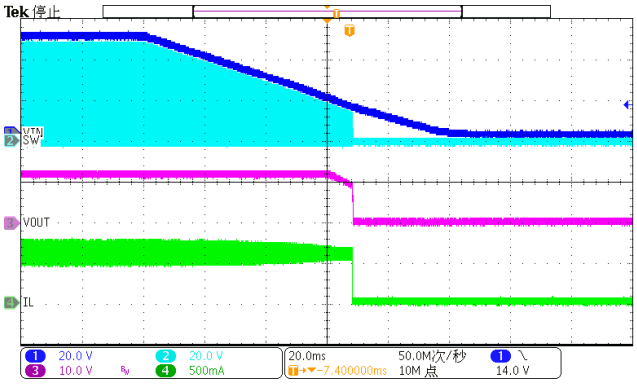

Figure 13. Power down

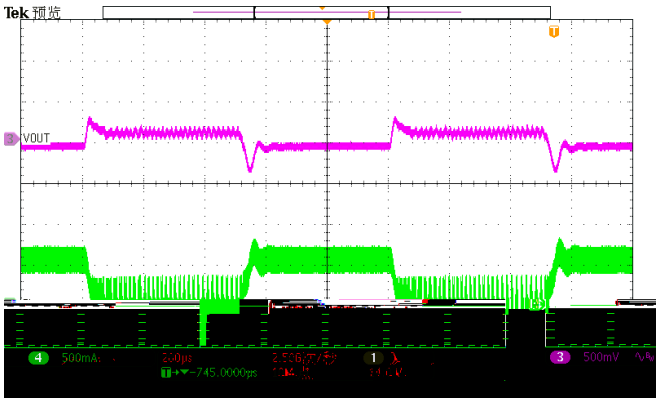

Figure 14.Load Transient (0.06A-0.54A, 0.25A/us)

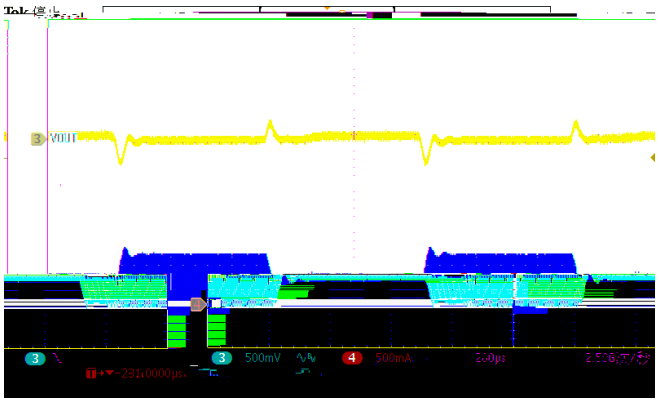

Figure 15. Load Transient (0.15A-0.45A, 0.25A/us)

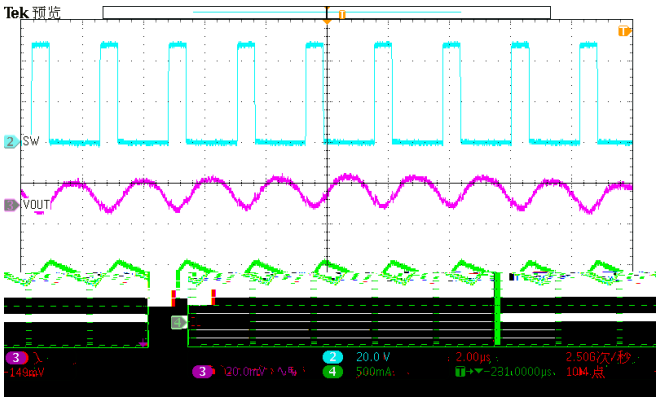

Figure 16. SW and Vout Ripple

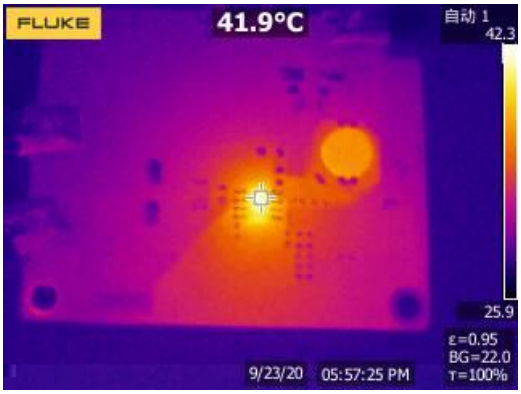

Figure 17. Thermal, 48VIN, 12Vout, 0.6A

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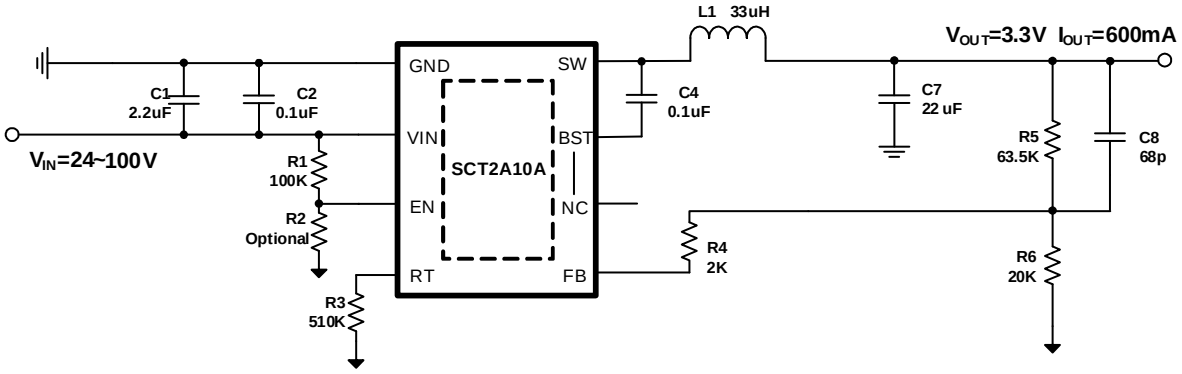

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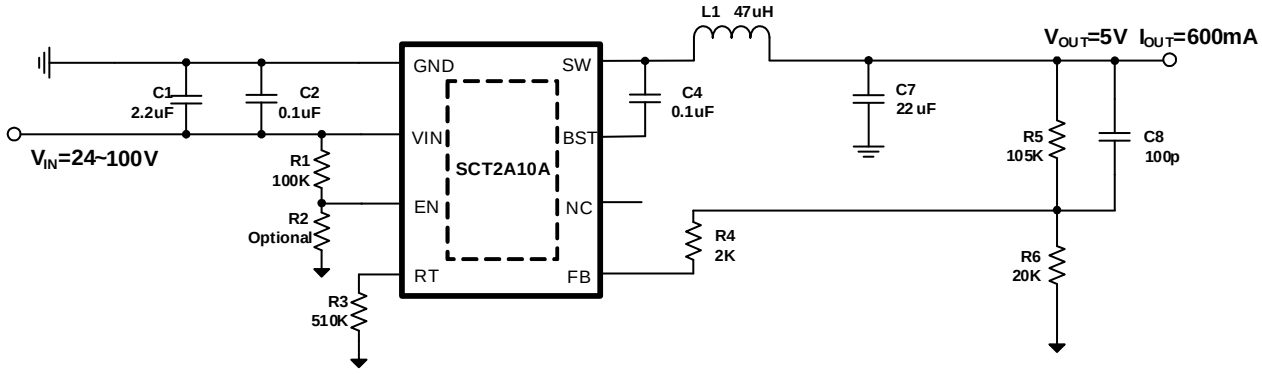

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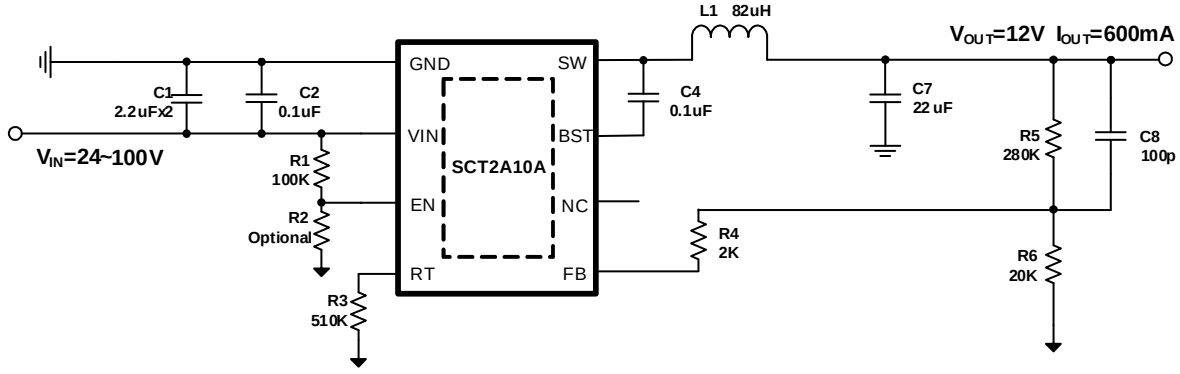


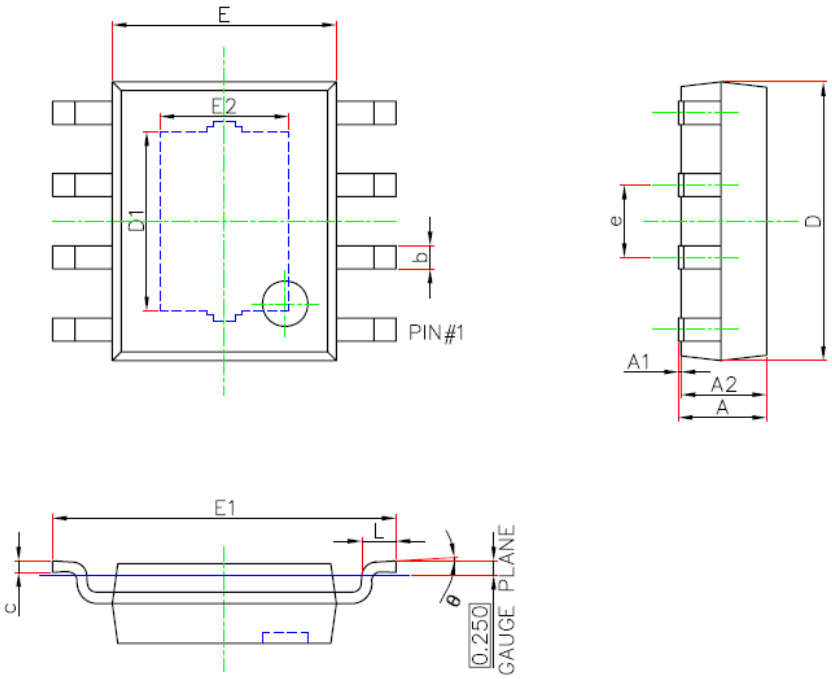
Bcc a , RKQP9 R EKQP9, 2= = e e e e

H C e a e a

Proper PCB layout is a critical for SCT2A10A's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. K Yfkkfd dXp i XdXi ifle gdXe fee k kfk ifle gdXe fekfg dXp i Yp mX The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be

PACKAGE INFORMATION



ESOP8/PP(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
	0°	8°	0°	8°

KPA6

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION